Remarks

This is a reply to the outstanding Office Action (first action on the merits), dated June 19, 2002, in which concurrently filed herewith is a Petition for Extension of Time covering the three-month extended time period for filing this response including the required fee amount thereto. (An authorized Credit Card Payment Form, covering the fee amount for the extended period of time, is enclosed herewith.)

A number of revisions to the Specification were implemented to correct noted informalities and/or improve the readability thereof. Several such minor revisions were implemented, also, in the Abstract. Since the changes effected are directed to minor formal matters, acceptance of the same is respectfully requested.

By the amendments presented hereinabove, independent claims 1 and 9 were revised to further clarify the subject matter intended to be covered and, also, with regard to avoiding any concerns such as that stated in the rejection under 35 USC §112, second paragraph. Specifically, with regard to each of independent claims 1 and 9, the expression "said glass substrate comprises an unannealed glass substrate" was substituted therefor by the phrase said glass substrate is such that its compaction is 30 ppm or higher, when said glass substrate is heated at 600°C for 1 hour and thereafter cooled at a rate of 1°C/minute. This revision to both base claim 1 and independent claim 9 is based on the related description found, for example, on page 5, lines 11-14 in the original Specification. Additional clarifications that are of a minor, formal matter were also implemented in each of independent claims 1 and 9. For example, the referred to "electrodes" in claims were deleted therefrom since it is understood that electrodes would be associated with the respectively corresponding source region and drain region of the thin-film transistor (TFT). It is submitted, in

view of the clarification effected in independent claims 1 and 9, reconsideration and withdrawal of that rejection, insofar as presently applicable to the remaining claims 1, 2, 9, and 11 and new claim 22, is respectfully requested.

By the Amendments presented hereinabove, additionally, original claims 3-8, 10 and 12 were canceled but, however, without prejudice or disclaimer of the subject matter therein, and claim 22 is being newly presented. The newly added claim 22, incidentally, was added to further highlight the type of structure that may be associated with the "first insulating layer" of the thin-film transistor according to claim 1. Incidentally, claim 1 now also specifically calls for a TFT scheme featuring a double-layer structure such as with regard to the gate insulator (e.g., gate insulating layer 6: 6a and 6b in Fig. 1), in which the "second insulating layer" is formed on a surface of the first insulating layer. Regarding the structural material associated with the "first insulating layer" (e.g., 6a in Fig. 1 in new claim 22), related discussion directed thereto is given on page 12, lines 15-23, in the Specification. Discussion will now turn to the art rejections.

It is noted that all of the art rejections include the qualification that they were made "insofar as [the claims were] in compliance with 35 USC §112." Specifically, claims 9-11 were rejected under 35 USC §102(b) over Yamazaki et al (US 6,025,630); claims 1-3 and 5-7 were rejected under 35 USC §102(b) over Abe et al (JP 8-195494); claim 12 was rejected under 35 USC §103(a) over the combination of Yamazaki et al (*supra)* in view of Yamazaki et al (US 6,168,980); claim 4 was rejected under 35 USC §103(a) over Abe et al *(supra)* in view of Yamazaki et al ('980); and claim 8 was rejected under 35 USC §103(a) over the combination of Abe et al *(supra)* in view of Tsutsu (US 6,118,151). Regarding the standing rejections of claims 3-8, 10 and 12, they have been rendered moot with the canceling of those

claims. As to the remaining claims 1, 2, 9, 11 and 22, the invention therein was neither taught nor suggested by any of the cited art documents, applied separately or, for that matter, in any combination. That is, it will be shown hereinbelow, the invention according to claims 1, 2 and 22 as well as that according to claims 9 and 11 could not have been achieved in the manner as that alleged in standing rejections directed thereto nor, for that matter, even if the teachings of the cited references were applied combinedly. Therefore, insofar as presently applicable, the rejections claims 1, 2 and 22 as well as that according to claims 9 and 11, are traversed and reconsideration and withdrawal of the same is respectfully requested.

In the TFT manufacturing schemes disclosed by Yamazaki et al ('630) and Abe, alkali-free glass such as Corning 7059 was used to form the glass substrate. Corning 7059, applicants submit, is often used as a heat-resistant glass substrate, noting that its distortion point is 593°C. Alkali-free glass substrates used as substrates of TFTs, typically, have a strain point of about 600°C, in which compaction (heat shrinkage) of glass becomes quite significant as a result of upper-end temperature changes. Regarding such glass substrates, it is also known that they cause compaction of about 200 ppm with a heating process at about 500°C for a glass substrate that was not annealed beforehand (in an unannealed state). The compaction with regard to glass substrate Corning 7059f not annealed beforehand is about 800 ppm with a heating process around 600°C, for 1 hour and at a cooling rate of 1°C/minute (see page 3, line 22, to page 4, line 3, of the specification). If, however, Corning 7059 becomes annealed with a heat process of about 650°C, the compaction is reduced to about 1/100th of the compaction caused by a heat process of about 500°C. This can be seen from Fig. 9 in the published article (see attached Reference 1) by M. Anma, entitled, "A New Measurement Method of Thermal

Dimensional Stability of Glass and Its Application to LCD Substrates." This illustration shows the relationship of the thermal shrinkage of the types of glass indicated including Corning 7059 employing such heat processes when it is in an unannealed state (previously not annealed) as well as when it is annealed.

It is also understood by one of ordinary skill that a permissible heat shrinkage rate (compaction) for a TFT substrate is less than 10 ppm and that glass whose compaction rate is 10 ppm and higher cannot be used as the TFT substrate. This is supported also from Table 3 of the attached Japanese language publication (see attached Reference 2). In fact, if in a substrate, a side thereof which is about 30 cm shrinks by 10 ppm, the amount of shrinkage thereof (e.g., 3 μm) would be comparable to that of a wiring width and can lead to loss of one of the wirings.

Accordingly, in Yamazaki et al ('630) and Abe in which a TFT substrate is manufactured, a heating process with a high temperature of about 600°C is executed in the manufacturing process in connection with the formation of a polysilicon TFT element having operating characteristics that are considerably improved over that of a known amorphous TFT element. As was shown hereinabove, since it becomes necessary to avoid heat shrinkage caused by such a heat process, it is apparent that unannealed Corning 7059 would not have been used with regard to the manufacture of either of Yamazaki et al's ('630) or Abe's TFT scheme. Rather, as was shown hereinabove, annealed Corning 7059 must have been used. That is, Corning 7059, described in the cited references, should have been annealed and, moreover, the compaction thereof, it is noted, is less than 30 ppm when heated at 600°C for 1 hour and thereafter cooled at a rate of 1°C/minute.

The present invention, however, is based on the breakthrough finding making it possible to manufacture a TFT substrate even when a glass substrate having high

compaction (in other words, a glass substrate that has not been previously annealed before a process) is used. This finding is achievable through focusing on the relationship between that of the physical property and temperature of the glass, wherein an element is formed in a temperature range within which the compaction of a glass substrate does not adversely affect the properties of a TFT element even when the TFT substrate is heated during the process.

According to the present invention, the "first insulating layer" which is formed on the glass substrate is either a silicon oxide layer or a silicon oxynitride layer (see claim 22), and a surface of the channel region is subjected to oxidization or oxynitridization with a temperature atmosphere of 500°C or lower. In this way, the TFT element can be made irrespective of the compaction characteristic of a glass substrate (i.e., even if an inexpensive unannealed glass is used), wherein the TFT element is formed with characteristic properties that are favorably compared with that manufactured using a high temperature process (about 600°C) using a conventional annealed glass.

Regarding the differences between claims 1 and 9, in claim 1, the thin-film transistor specifically calls for a "first insulating layer" covering the channel region of the TFT and also a "second insulating layer" formed on a surface of the first insulating layer such as shown by the example embodiment in Fig. 1 of the drawings, although not limited thereto. On the other hand, the invention according to claim 9, as it relates to the gate insulator, specifically calls for an "insulating layer" which covers the channel region (e.g., see double - layer gate insulator 6 in Fig. 1 and the single-layer insulator 6 in Fig. 4, although not limited thereto). The invention according to claims 1 and 9 having a polycrystalline silicon layer formed under low-temperature processing conditions and yet employing a glass substrate as that

presently called for that was previously not annealed, was neither disclosed nor suggested by Yamazaki et al ('630) nor by Abe, these disclosures taken separately or, for that matter, in combination.

Also according to the present invention, the first insulating layer of the gate insulator is formed to be at least 4 nm. As a result, therefore, the phenomenon of the interfacial state density at the interface between that of insulating layer and the underlying silicon layer is significantly lower which leads to an improvement in the characteristics of the TFT elements (See claim 2). In contradistinction with that called for in claim 2, Abe's insulating layer 3, as stated in the Office Action, has a thickness (range) of 5 to 10 nm. 4 nm, it is noted, is significantly lower than 5 nm in terms of the lower limit of the range and, moreover, the present invention is not necessarily limited to Abe's upper range in the thickness of the first insulating layer. Although the featured aspects called for in dependent claim 2 and, for that matter, with regard to claims 11 and 22 are not necessary to establish patentability of the present invention over the teachings of Yamazaki et al ('630) and Abe, taken separately or in combination, they are illustrative of additional patentable differences therefrom, although not limited thereto.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, favorable action therefor on the presently pending claims, i.e., claims 1, 2, 9, 11 and 22, and an early formal Notification of Allowability of the above-identified application is respectfully requested.

A marked-up version showing changes made is enclosed herewith.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of

Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (566.40894X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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Attachments: Mark-up Version Showing Changes Made
Reference 1
Reference 2

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MARKED-UP VERSION SHOWING CHANGES MADE

IN THE SPECIFICATION:

On Page 3, please amend the third paragraph, beginning at line 7, as follows:

According to the above method disclosed in Japanese Patent Application Laid-open No. 8-195494, since the polycrystalline silicon layer is formed at a temperature of about 600°C, a usable glass substrate is limited to an annealed glass substrate. Hence, when an unannealed glass substrate is used in place of the annealed glass substrate, the temperature condition of about 600°C may cause a shrinkage of the glass substrate, and this may cause a warpage or strain of the glass substrate to bring about difficulties such as break of the glass substrate itself and peel of the layer [in the], at worst.

On Page 3, please amend the last paragraph, beginning at line 22 and bridging to page 4, line 8, as follows:

Usually, alkali-free glass substrates used as substrates of thin-film transistors have a strain point of about 600°C, and compaction (heat shrinkage) of glass becomes great abruptly as a result of heat history at upper temperatures than at a temperature a little lower than the strain point. For example, an unannealed glass substrate CORNING 7059F (Trade name: available from Corning Glass works; strain point 593°C) shows a compaction of about 800 ppm as a result of heat history at 600°C, for 1 hour and at a cooling rate of 1°C/minute. Also, in the case of CORNING 1735F (strain point: 665°C), having a higher strain point, it shows a compaction of 173 ppm upon application of the same heat history as the above. Then, it has been

made possible to lower compaction due to the like heat history to about 10 ppm by carrying out annealing previously at 660°C/1 hr.

On Page 4, please amend the last paragraph, beginning at line 17, as follows:

That is, as a gate-insulating layer formed on a polycrystalline silicon layer, as stated previously an SiO_2 layer is formed in a layer thickness of about 100 nm by plasma-assisted CVD (chemical vapor deposition) using TEOS (tetraethoxysilane) as a material gas (herein "TEOS layer"). At the interface between the polycrystalline silicon layer and the insulating layer formed of TEOS, however, the interfacial density of the TEOS layer [has so high an interfacial state density is] becomes so high that the threshold voltage required [as] of a TFT tends to vary and also the breakdown strength [required as] of the gate-insulating layer thereof may severely deteriorate with time. Thus, there is a great problem on the reliability of TFT.

On Page 5, please amend the third paragraph, beginning at line 15, as follows:

To achieve the above object, in the present invention, i) a polysilicon crystal layer for forming a channel region, a source region and a drain region and ii) a first [insulting] insulating layer and a second insulating layer are formed at the upper part of an unannealed glass substrate. Also, a gate region is formed at a position corresponding to the channel region and on the second insulating layer. And a gate electrode, a source electrode and a drain electrode are also formed to make electrical interconnection with the gate region, the source region and the drain region, respectively.

On Page 5, please amend the last paragraph, beginning at line 24, and bridging to page 6, line 1, as follows:

Here, it is preferable that the first insulating layer is a silicon oxide layer formed by oxidizing the surface of the channel region at a temperature of 500°C or below, and is so formed as to cover the surface of at least the channel region and to [be in] have a layer thickness of 4 nm or larger.

On Page 6, please amend the first full paragraph, beginning at line 2, as follows:

In the present invention, it is preferable that the first insulating layer, e.g., a silicon oxide layer, is formed by oxidizing the surface of a polycrystalline silicon layer in an atmosphere containing at least ozone, for example, an atmosphere containing ozone and H_2O or an atmosphere containing ozone and N_2O. Also, in the present invention, in the step of forming the first insulating layer, it is preferable that a first silicon oxide layer is formed at the surface of the polycrystalline silicon layer by the use of an oxygen-donating solution, and thereafter a second silicon oxide layer is formed between the first silicon oxide layer and the polycrystalline silicon layer in an atmosphere containing ozone.

On Page 6, please amend the last paragraph, beginning at line 22, and bridging to page 7, line 4, as follows:

In other words, the thin-film transistor manufactured by the above method has a good interface between the surface of the channel region comprised of polycrystalline silicon and the gate insulating layer formed thereon, and hence the thin-film transistor characteristics concerned closely with the interfacial state density thereat, as exemplified by threshold voltage, can be made to [less] vary less, so that

superior TFT characteristics can be exhibited. In addition, since the unannealed glass substrate can be used as the substrate, the TFT can be formed in a large area and at a low cost, compared with quartz glass substrates or the like.

On Page 7, please amend the second paragraph, beginning at line 5, as follows:

In the above means for solving the problem, the insulating layer has a double-layer structure, which, however, need not necessarily be [the double-layer structure] limited thereto.

On Page 7, please amend the fifth paragraph, beginning at line 15, as follows:

Figs. 2A to 2D show [a] flow [sheet] diagrams for describing various stages of a process of manufacturing the thin-film transistor according to a first embodiment;

On Page 7, please amend the last paragraph, beginning at line 24, as follows:

Fig. 7 is a schematic view for describing changes in surface temperature of a silicon substrate in an embodiment[;].

On Page 8, please amend the fourth paragraph, beginning at line 18, as follows:

A method of producing the above structure shown in Fig. 1 is described below with reference to [a] the flow diagrams shown in Figs. 2A to 2D.

On Page 10, please amend the last paragraph, beginning at line 21, and bridging to page 11, line 2, as follows:

Incidentally, although it is unnecessary to [dare to define the] specifically set an upper limit of the thermal-oxide layer thickness, [but it is unnecessary to make its] the` thickness need not be made to large [too much] when the gate insulating layer is formed in the thermal oxide/TEOS double-layer structure. More specifically, taking account of the productivity of thin-film transistors, it is suitable for the layer thickness to be, e.g., about 20 nm in maximum, considering that the process of thermal oxidation is a process in which the oxide layer is formed at a low rate.

On Page 11, please amend the first full paragraph, beginning at line 3, as follows:

In the above first embodiment, described is a case in which the gate-insulating layer 6 has a double-layer structure. It may also [has] have a single-layer structure as shown in Fig. 4. In the latter case, the step of forming the second insulating layer 6b may only be omitted in the steps described above.

On Page 13, please amend the third full paragraph, beginning at line 9, as follows:

As a method of forming the oxide layer of about 1 nm in layer thickness, for example, a sample on which the polycrystalline silicon layer 4 has been formed may be immersed [in,] in ozone water prepared by bubbling ozone gas into pure water. Also, in place of the ozone water, the sample may be immersed in an aqueous ammonia/hydrogen peroxide solution.

On Page 15, please amend the third paragraph, beginning at line 12, as follows:

In order to accelerate the oxidation reaction at the substrate surface, it is necessary to prevent the ozone itself from decomposing and the temperature of the substrate surface from lowering, in the course before the ozone reaches the surface of the substrate. In other words, it is preferable to keep the temperature at 200°C or below, and more preferably 150°C or below, which is a temperature of such a degree that the ozone gas fed to the surface of the substrate does not decompose, and also to keep only the substrate surface at a high temperature.

On Page 15, please amend the last paragraph, beginning at line 25, and bridging to page 26, line 6, as follows:

In general, where a gas is fed to the surface of a substrate in the state the substrate is held on a stage the temperature of which is controlled by means of a general-purpose heater, the temperature of the substrate surface changes as shown in Fig. 5. More specifically, in Fig. 5, the lapse of time is plotted as [ordinate] abscissa, and the input to a heater, the internal temperature of a stage to which the heater is attached and the surface temperature of the substrate are plotted as ordinate, showing changes of the surface temperature of the substrate.

On Page 18, please amend the last paragraph, beginning at line 26, and bridging to page 19, as follows:

While we have shown and described several embodiments in accordance with our invention, it should be understood that disclosed embodiments are susceptible of changes and modifications without departing from the scope of the invention. Therefore, we do not intend to be bound by the details shown and described herein

but intend to cover all such changes and modifications [a] that fall within the ambit of the appended claims.

IN THE CLAIMS:

Please **amend** claims 1, 2 and 9, as follows:

1. (Amended) A thin-film transistor comprising:

a glass substrate; and

formed at an upper part of said glass substrate, a channel region, a source region, a drain region, a first insulating layer[,] and a second insulating layer [and electrode], wherein:

said channel region, said source region and said drain region comprise polycrystalline silicon,

said glass substrate [comprises an unannealed glass substrate] is such that its compaction is 30 ppm or higher, when said glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute, [and]

said first insulating layer covers said channel region, and

said second insulating layer is formed on a surface of said first insulating layer.

2. (Amended) The thin-film transistor according to claim 1, wherein said first insulating layer has a layer thickness [of] whose lower limit is 4nm [or larger].

9. (Amended) A thin-film transistor comprising:

a glass substrate; and

formed at an upper part of said glass substrate, a channel region, a source region, a drain region[,] and an insulating layer [and electrodes], wherein:

said channel region, said source region and said drain region comprise polycrystalline silicon,

said glass substrate [comprises an unannealed glass substrate] is such that its compaction is 30 ppm or higher, when said glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute, and

said insulating layer covers said channel region.

IN THE ABSTRACT:

Please **replace** the Abstract with the amended Abstract, as follows:

To a polycrystalline silicon layer crystallized by irradiation with laser light, a mixed gas comprises of ozone gas and H_2O or N_2O gas is fed at a processing temperature of 500°C or below, or the polycrystalline silicon layer is previously treated with a solution such as ozone water or an aqueous NH_3/hydrogen peroxide solution, followed by oxidation treatment with ozone, to form a silicon oxide layer with a thickness of 4 nm or more [thick] at the surface of the polycrystalline silicon layer for forming a thin-film transistor having [less variations of] characteristics that are less varying on [an unannealed] a glass substrate previously not annealed.